THAT WHICH IS CLAIMED IS:

1. An integrated circuit device, comprising:

an integrated circuit substrate having a fuse region;

a window layer on the integrated circuit substrate defining the fuse region, the window layer positioned at an upper portion of the integrated circuit device and recessed beneath a surface of the integrated circuit device;

a buffer pattern between the integrated circuit substrate and the window layer; and

a fuse pattern between the buffer pattern and the window layer.

2. The integrated circuit substrate of Claim 1, further comprising a metal wiring on the integrated circuit substrate wherein the window layer is more remote from the integrated circuit substrate than the metal wiring.

3. The integrated circuit device of Claim 1, wherein the buffer pattern comprises a first buffer pattern, the device further comprising:

a first insulation layer between the first buffer pattern and the fuse pattern;

a second buffer pattern between the first buffer pattern and the integrated circuit substrate; and

a second insulation layer between the second buffer pattern and the first buffer pattern.

4. The integrated circuit device of Claim 3, wherein the fuse pattern comprises a first conductive material, the first buffer pattern comprises a second conductive material and the second buffer pattern comprises a third conductive material, wherein the second and third conductive materials are different from the first conductive material and wherein the first and second buffer patterns are planar.

5. The integrated circuit device of Claim 4, wherein the first conductive material comprises aluminum, tungsten and/or copper, wherein the second conductive material comprises polysilicon, ruthenium, platinum, iridium, titanium nitride, tantalum nitride and/or tungsten nitride and wherein the third conductive material comprises polysilicon, ruthenium, platinum, iridium, titanium nitride, tantalum nitride and/or tungsten nitride.

6. The integrated circuit device of Claim 3, further comprising:

a line pattern between the integrated circuit substrate and the second insulation layer adjacent the second buffer pattern;

a contact hole in the first and second insulation layers; and

a contact plug in the contact hole that electrically couples the fuse pattern to the line pattern.

7. The integrated circuit device of Claim 3, further comprising:

a conductive layer pattern between the second insulation layer and the first insulation layer adjacent the first buffer pattern;

a third insulation layer on the first insulation layer and the fuse pattern;

a metal wiring on the third insulation layer above the conductive layer pattern, wherein the first and third insulation layers define a via hole therein;

a conductive plug in the via hole that electrically couples the conductive layer pattern and the metal wiring.

8. The integrated circuit device of Claim 3 wherein the integrated circuit device comprises an integrated circuit memory device.

9. A method of forming an integrated circuit device, comprising:

forming a window layer on an integrated circuit substrate that defines a fuse region such that the window layer is formed at an upper portion of the integrated circuit device and recessed beneath a surface of the integrated circuit device;

forming a buffer pattern between the integrated circuit substrate and the window layer; and

forming a fuse pattern between the buffer pattern and the window layer.

10. The method of Claim 9, further comprising forming a metal wiring on the integrated circuit substrate, the metal wiring being more remote from the integrated circuit substrate than the window layer.

11. The method of Claim 10, wherein forming the buffer pattern comprises forming a first buffer pattern, the method further comprising:

forming a first insulation layer between the first buffer pattern and the fuse pattern;

forming a second buffer pattern between the first buffer pattern and the integrated circuit substrate; and

forming a second insulation layer between the second buffer pattern and the first buffer pattern.

12. The method of Claim 11, wherein forming the window layer comprises:

forming a third insulation layer on the first insulation layer;

forming a passivation layer on the third insulation layer;

etching the passivation layer and the third insulation layer in the fuse region to the window layer on the fuse pattern that is recessed beneath the surface of the integrated circuit device.

13. The method of Claim 11, wherein forming the fuse pattern comprises forming a fuse pattern comprising a first conductive material, wherein forming the first buffer pattern comprises forming the first buffer pattern comprising a second conductive material, wherein forming the second buffer pattern comprises forming a second buffer pattern comprising a third conductive material, wherein the second and third conductive materials are different from the first conductive material and wherein the first and second buffer patterns are planar.

14. The method of Claim 11, further comprising:

forming a line pattern between the integrated circuit substrate and the second insulation layer adjacent the second buffer pattern;

forming a contact hole in the first and second insulation layers that exposes a portion of the line pattern; and

forming a contact plug in a contact hole that electrically couples the fuse pattern to the line pattern.

15. The method of Claim 11, further comprising:

forming a conductive layer pattern between the second insulation layer and the first insulation layer adjacent the first buffer pattern;

forming a third insulation layer on the first insulation layer and the fuse pattern;

forming a metal wiring on the third insulation layer above the conductive layer pattern;

forming a via hole in the first and third insulation layers that exposes at a portion of the conductive layer pattern; and

forming a conductive plug in a via hole that electrically couples the conductive layer pattern and the metal wiring.

16. The method of Claim 11, wherein forming the integrated circuit device comprises forming an integrated circuit memory device.

17. A method of forming an integrated circuit device, comprising:

forming a conductive layer on an integrated circuit substrate, the conductive layer extending from a cell region to a fuse region of the integrated circuit substrate;

patterning the conductive layer to simultaneously form a plate electrode in the cell region and a buffer pattern in the fuse region;

forming a first insulation layer on the plate electrode and the buffer pattern;

forming a metal layer on the first insulation layer that extends from the cell region to the fuse region;

patterning the metal layer to simultaneously form a metal wiring in the cell region of the integrated circuit substrate and a fuse pattern in the fuse region of the integrated circuit substrate;

forming a second insulation layer on the metal wiring and the fuse pattern;

forming a passivation layer on the second insulation layer; and

etching the passivation layer and the second insulation layer in the fuse region of the integrated circuit substrate to form a window layer defining the fuse region.

18. The method of Claim 17, wherein forming a conductive layer comprises forming a first conductive layer and wherein forming the buffer pattern comprises forming a first buffer pattern, the method further comprising:

forming a second conductive layer on the integrated circuit substrate extending from the cell region to the fuse region, the second conductive layer being positioned between the integrated circuit substrate and the first buffer pattern; and

patterning the second conductive layer to simultaneously form a bit line in the cell region and a second buffer pattern in the fuse region.

19. The method of Claim 18, wherein forming the second conductive layer further comprises:

forming a first layer of conductive material on the integrated circuit substrate;

forming a second layers of conductive material on the first layer of conductive material; and

etching the first and second layer of conductive material to simultaneously form the bit line and the second buffer pattern.

20. The method of Claim 19 wherein the first layer of conductive material comprises polysilicon and the second layer of conductive material comprises tungsten silicide.

21. The method of Claim 18, further comprising forming a third insulation layer between the second buffer pattern and the first buffer pattern.

22. The method of Claim 21 wherein forming the first buffer pattern comprises:

forming an fourth insulation layer on third insulation layer in the fuse region of the integrated circuit substrate; and

etching the first conductive layer such that a portion of the first conductive layer remains on the fourth insulation layer in the fuse region of the integrated circuit substrate.

23. The method of Claim 17, wherein forming the metal wiring and the fuse pattern comprises:

forming a first layer of a metal on the first insulation layer;

forming a second layer of a metal compound on the first layer;

forming a photoresist pattern on the first and second layers;

etching the first and second layers according to the photoresist pattern to simultaneously form the metal wiring and the fuse pattern.

24. The method of Claim 18 wherein forming an integrated circuit device comprises forming an integrated circuit memory device.

25. The method of Claim 24 wherein the integrated circuit memory device comprises a dynamic random access memory (DRAM) device.